What is claimed is:

1. A method for analyzing an integrated circuit die, the method comprising:

removing substrate from a selected portion of the die;

simultaneously recording a plurality of images of the selected portion as substrate is being removed therefrom; and

creating a three-dimensional image of the selected portion of the die with the plurality of images and analyzing the die therefrom.

2. The method of claim 1, wherein removing substrate includes cross-sectioning the die.

3. The method of claim 1, wherein removing substrate includes using a FIB.

4 The method of claim 1, wherein recording a plurality of images includes using a SEM.

5. The method of claim 1, wherein removing substrate includes using a FIB produced by a dual FIB/e-beam device, and wherein recording a plurality of images includes using the e-beam of the dual FIB/e-beam device to create a SEM image.

6. The method of claim 5, further comprising programming a controller adapted to control the dual FIB/e-beam device to effect the recording of a sufficient amount of SEM images to create a three-dimensional image of the selected portion.

7. The method of claim 1, wherein removing substrate from the selected portion includes exposing a defect in the die, and wherein creating a three-dimensional image includes creating a three-dimensional image of the defect.

8. The method of claim 1, wherein creating a three-dimensional image includes combining the plurality of images of the selected portion and creating a combined image therefrom.

9. The method of claim 1, further comprising using the three-dimensional image to detect a defect in the die.

10. The method of claim 9, wherein creating a three-dimensional image includes creating an image of the defect, further comprising using the image of the detected defect to analyze the defect.

11. The method of claim 1, wherein creating a three dimensional image includes using selected ones of the plurality of images of the selected portion to create a three dimensional image of less than the entire selected portion.

12. The method of claim 1, further comprising editing the three dimensional image to create an edited image of only a portion of the three-dimensional image.

13. The method of claim 12, wherein editing the three-dimensional image includes creating an image of a cross-section of the selected portion.

14. A system for analyzing an integrated circuit die, the system comprising:

means for removing substrate from a selected portion of the die;

means for simultaneously recording a plurality of images of the selected portion while substrate is being removed therefrom; and

means for creating a three-dimensional image of the selected portion of the die with the plurality of images.

15. A system for analyzing an integrated circuit die, the system comprising:

a substrate removal arrangement adapted to remove substrate from a selected portion of the die;

an image recording arrangement adapted to simultaneously record a plurality of images of the selected portion while substrate is being removed therefrom; and

an image creation arrangement adapted to create a three-dimensional image of the selected portion of the die with a plurality of images recorded by the imaging arrangement.

16. The system of claim 15, wherein the substrate removal arrangement includes a FIB device

17. The system of claim 15, wherein the image recording arrangement includes an e-beam device adapted to create a SEM image.

18. The system of claim 15, wherein the substrate removal arrangement and the image recording arrangement are included in a single dual FIB/e-beam device adapted to remove substrate with the FIB and to create a SEM image with the e-beam.

19. The system of claim 18, wherein the image creation arrangement is adapted to use the SEM image to create the three-dimensional image.

20. The system of claim 15, wherein the image creation arrangement includes a computer adapted to create the three-dimensional image in response to image characteristic selections.